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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/465,634	12/17/1999	DAVID K. VAVRO	INTL-0286-US	9115

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/465,634	VAVRO ET AL.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 8-10, 14, 15, 16, 17, 22, 23, and 24 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Renner et al., US Patent 4,75,544.

3. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, mailed on February 8, 2005.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Renner et al., US Patent 4,75,544.

6. Claims 11-13, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Renner et al., US Patent 4,75,544, in view of Nakagawa et al., U.S. Patent Number 5,241,679 (hereinafter Nakagawa).

7. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, mailed on February 8, 2005.

Response to Arguments

8. Applicant's arguments filed April 15, 2005 have been fully considered but they are not persuasive.

On page 2, Applicant argues with respect to claim 1 in essence:

"The office action indicates that the input processor is the element 12 in Figure 1, but it is respectfully submitted that this could not possibly be the case because, as shown in Figure 1, the1/0 port is on the lower right hand of the figure and is nowhere close to the item 12. Thus, it is clear that the item 12 does not process input signals. The item 12 is an array controller and sequencer which operates as the master of the array processor and controls the instruction flow therein."

However, the processor, element 12, does in fact process input signals. Input signals for processing are provided to element 12 via elements 26 and 50 and from the external device control in Figure 3. See column 6, lines 45-56, column 7, lines 15-17, and column 7, lines 50-55. Therefore element 12 is in fact an input processor that processes input signals. Therefore this argument is moot.

9. On page 2, Applicant argues with respect to claim 1 in essence:

"The office action suggests that the output processor is the element 20a but, again, this cannot be so because, again, the 1/0 port is in the bottom right hand corner of the figure and is nowhere close to the item 20a. Instead, the item 20a is described at column 3, lines 29-31, as a vector address generator. A vector address generator is not a processor which processes output signals from the digital signal processor."

However, element 20a is a processor which processes output signals from the digital signal processor. Output signals for processing are provided to element 20a via elements 18 and 26. See column 7, line 55-column 8, line 52. The output signals come from the digital signal processor, specifically from elements 12 and 24. So element 20a is in fact

an output processor that processes output signals from the digital signal processor.

Therefore this argument is moot.

10. On page 2, Applicant argues with respect to claim 1 in essence:

"Finally, it is suggested in the office action that the storage selectively accessible by each of the processors is the external ROM, citing column 3, lines 23-26. However, the external ROM is not indicated as being accessible by each of the processors. Each of the processors would be the programmable, multiply and accumulate mathematical processor, the input processor, the output processor, and the master processor. Nothing in the cited material suggests that the ROM is accessible by anything other than the ACS 12. Note that the items 20a, 20b, and 20n have their own separate code section indicated as microcode 30. Thus, if the Examiner still believes that these items are the output processor, there is no reason to believe that they have any way of accessing the so-called external ROM which is the item 40. In addition, the array controller 12 has its own microcode storage 14. There is no reason to believe that the microcode 14 is accessible by anything other than the array controller."

However, each processor has a ROM, either internal or external to the processors, for element 12 see column 3, lines 23-26, for element 20a see column 8, lines 1-13, for element column 9, lines 45-58, and column 3, lines 50-57. All of the ROM's for each processor together comprise the claimed storage selectively accessible by each of the processors.

11. On page 3, Applicant argues in essence:

"Claim 2 calls for a random access memory processor that stores intermediate calculation results. It is suggested in parapaph 4 of the office action that this is the element 20b. However, nothing indicates that the code store 30 is randomly accessible. Since what is stored there is microcode 30, there is no particular reason to believe that it is randomly accessible. At line 37 of column 3, the microcode 30 is called CCROM resident." This would further suggest that it is not randomly accessible."

However, the entire citation for claim 2 in paragraph 4 of the last office action is "(Figure 1, element 20b, Figure 4, element 202)". Figure 4 is a detailed illustration of element 20b. Inside element 20b is element 202. Element 202 is a Parameter Register File,

which is a RAM to store intermediate results. Therefore element 20b is a random access memory processor that stores intermediate results. Therefore this argument is moot.

12. On page 3, Applicant argues in essence:

" Claim 3 calls for a bus coupling each of said processors to the storage. The office action does not point out where such buses might possibly be. Therefore, reconsideration is respectfully requested."

However, each processor has a ROM, either internal or external to the processors, for element 12 see column 3, lines 23-26, for element 20a see column 8, lines 1-13, for element column 9, lines 45-58, and column 3, lines 50-57. All of the ROM's for each processor together comprise the claimed storage selectively accessible by each of the processors. In order for the processors to access the data in the storage, there must be a bus coupling each processor to said storage. Therefore this argument is moot.

13. On page 3, Applicant argues in essence:

"Concerning claim 4, since there are no input and output processors, there are no such processors that implement mathematical operations."

However, there are input and outputs processors. See the arguments above and the rejection to claim 1. Therefore this argument is moot.

14. On page 3, Applicant argues in essence:

"With respect to claim 5, it is suggested in the office action that the Abstract indicates that each of the asserted processors have their own instruction sets. However, all that the Abstract indicates is that data instructions are sequenced through in accordance with sequenced commands by the master controller 12. This does not suggest that each of the so-called processors have instructions, much less their own instruction sets. Therefore, reconsideration is requested."

However, each processor executes a set of commands, or instructions. A set of instructions being executed by a specific processor is the instruction set for the specific

processor. For example, a set of instructions being executed in element 10 is the instruction set for element 10, a set of instructions being executed in element 12 is the instruction set for element 12, a set of instructions being executed in element 20a is the instruction set for element 20a, a set of instructions being executed in element 24 is the instruction set for element 24. So Renner et al. has in fact taught wherein each of said processor have their own instruction sets. Therefore this argument is moot.

15. On page 3, Applicant argues in essence:

"Claim 6 calls for each of the processors to communicate with one another through said storage. The material at column 3, lines 23-26, does not describe such a communication system."

However, in Renner et al. communication is throughout the entire system, including the claimed storage. See Figure 1. Therefore, Renner et al. have in fact taught wherein said processors communicate with one another through said storage. Therefore this argument is moot.

16. On page 3, Applicant argues in essence:

"Claim 8 calls for each of the processors to receive timing from the master processor. The material cited in support thereof column 3, lines 13-25, does not discuss any kind of timing. Therefore, reconsideration is requested."

However, in Renner et al. the master processor determines the timing for when the processors execute instructions because it controls when the instructions are sent to each individual processor. The timing of when the instructions begin executing in each of the processors is provided by the master processor sequencer, see column 3, lines 13-25. Therefore this argument is moot.

17. On page 3, Applicant argues in essence:

"Claim 9 calls for the master processor to wait for the input processor to complete a given operation. It is suggested that it is inherent because the system is clocked. Just because a system is clocked does not mean that it needs to be sequential in the fashion claimed. Therefore, reconsideration is requested."

However, claim 9 calls for the master processor to wait for the input processor to complete a given operation. In the case of a clocked system, the master processor sends an instruction on a clock signal. The master processor waits for the next clock signal to send another instruction. The given operation as claimed is the input processor executing for at least one clock cycle. The master processor waits for the input processor to complete one clock cycle before possibly sending another instruction to the processor. So Renner et al. have in fact taught wherein said master processor waits for the input processor to complete a given operation as claimed. Therefore this argument is moot.

18. On pages 3 and 4, Applicant argues in essence:

"Claim 10 calls for each of the processors to have its own random access memory. It is suggested that Renner teaches this, citing element 132 of Figure 4 and element 202 of Figure 5, element 220 and inherent in element 10. The element 132 is described at column 6, lines 54-56. Nothing indicates that it is randomly accessible. The item 202 is described as a parameter register file at lines 34 and 35 of column 8. However, nothing indicates that it is randomly accessible. Similarly, nothing indicates that the element 220 is randomly accessible. The item 220 is a multiplier file and it is not even seen why it would be believed that it would be randomly accessible. It is suggested that the item 10 is inherently randomly accessible. However, it is not seen why this is so. The only discussion of any stored code is ROM stored code which would not be randomly accessible. Therefore, reconsideration of the rejection of claim 10 is respectfully requested."

However, random access memory, or RAM, is defined as memory that can be written to as well as read. Figure 3, Element 132, Figure 4, element 202, and Figure 5, element 220, can all be written to as well as read, so the elements are all random access memories. Therefore each processor has it's own random access memory and this argument is moot.

19. On page 4, Applicant argues in essence:

In the present application, a multi-cycle arithmetic element uses a busy signal to hold off new data from being sourced to the arithmetic element 98. See page 24 of the specification at lines 15-19. Thus, it does not appear that anything in the cited reference constitutes a multi-cycled mathematical processor set forth in claim 15. Therefore, reconsideration is requested.

However, Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978). In this case, a multi-cyled mathematical processor is interpreted as a processor that has operations that take multiple cycles to complete execution. The mathematical processor is pipelined, so operations executed in the mathematical processor take multiple cycles to complete (column 14, lines 58-61, Figure 5, element 24). So element 24 is in fact a multi-cycled mathematical processor. Therefore this argument is moot

20. On page 4, Applicant argues in essence:

"Claim 7 was rejected as obvious over Renner taken alone. It is not understood how a single reference could establish a prima facie obviousness rejection. Necessarily, the reference is missing something and it cannot teach that very missing thing. While arguments are made about how good it would be to have very long instruction words in Renner, there is no reason to believe that Renner could have accommodated very large instruction words or that he ever thought to use them. Therefore, a prima facie rejection cannot be made out because nothing in Renner suggests the use of very long instruction words."

However, Referring to claim 7, Renner et al. have taught the digital signal processor of claim 1, as described above. Renner et al. have not specifically taught wherein each of said processors use very long instruction words. Employing this type of instruction format is well known in the art and would have allowed for the processors of Renner et

al. to issue several instructions at once and ensured, by the nature of VLIW instructions, that the compiler would have only combined instructions that are not dependent upon one another (see Hennessy pages 278-279 for extrinsic evidence of this fact). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the very long instruction word format for instructions issued to the plural processors of Renner et al. in order to increase speed and efficiency of those processors by issuing more instructions at once. Official notice was taken in the last office action, and in the instant office action Hennessy is cited for support. Therefore this argument is moot.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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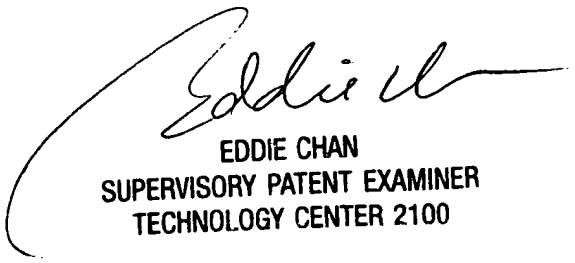

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